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(54) Title: SYSTEM AND METHOD FOR DEPOSITING INORGANIC/ORGANIC DIELECTRIC FILMS

(57) Abstract: A system and method for depositing a dielectric film on the surface of a substrate is provided having a processing chamber with a substrate support for supporting a substrate and one or more gas inlets for conveying gases to the processing chamber. A first plasma source defining a first plasma zone within the chamber is provided, and a second plasma source defining a second plasma zone within said chamber is provided. Gases are separately ionized at different ionization levels in the first and second plasma zones, and these separately ionized gases react to form a dielectric film on the surface of the substrate.

# SYSTEM AND METHOD FOR DEPOSITING INORGANIC/ORGANIC DIELECTRIC FILMS

## Cross-Reference to Related Applications

This patent application claims the benefit of US provisional patent application Serial No. 60/166,662 filed on November 19, 1999, the entire disclosure of which is herein incorporated by reference.

## Field of the Invention

This invention relates to a system and method for depositing oxide films, and more particularly to a system and method for depositing inorganic/organic oxide films having a low dielectric constant (κ) on the surface of a substrate.

## Background of the Invention

One of the greatest challenges for the microelectronics industry in the coming years is the identification of advanced dielectric materials that can replace silicon dioxide as an inter and intra metal layer dielectric. Dielectric film layers are fundamental components of integrated circuits and semiconductors. Such films provide electrical isolation between components. As device densities increase, multiple layer dielectric films are generally used to isolate device features. When forming dielectric films it is important for the film to exhibit certain properties, such as good gap fill, thermal stability and favorable electrical properties. The most widely used dielectric layer, silicon dioxide ($SiO_2$) is formed by a variety of methods. The most commonly used methods are chemical vapor deposition (CVD), plasma CVD, and spin-on coating.

The key driver for seeking increasing device densities is faster operating speeds. The shorter the distance between elements of the integrated circuit, the faster the signals can be transmitted. However, as device densities increase and the gaps between lines become smaller, the demands on the insulating films become more rigorous. When the critical feature size decreases below about 0.25 microns, the dielectric constant (κ) of the insulating dielectric material acquires increasing importance. Specifically, the dielectric constant determines the

capacitance of the device and thus also influences; (a) the capacitive interconnect delays, (b) crosstalk, which can result in errors in signal transmission, and (c) the power consumption. All of these influences are minimized by lowering the dielectric constant of the insulating material.

For highest transmission speeds, the capacitive interconnect, or RC, delays must be minimized. There are generally two ways to reduce the RC delay for a given device. The first is to reduce the resistance of the interconnect lines by using different metals. The second way is to reduce the dielectric constant by modifying or using different dielectric material. Both avenues have been pursued in the prior art, with the first having but one alternative (copper), and the second having numerous alternative approaches.

Currently, devices may incorporate five or six dielectric layers, all comprised of silicon dioxide. Replacing $SiO_2$ with a suitable low dielectric constant (low $\kappa$) material will thus lead to a dramatic improvement in speed and reduction in the power consumption of the device.

The lowest possible dielectric constant is 1.0 (dielectric constant of vacuum) while silicon dioxide, $SiO_2$, has a dielectric constant of about 3.9 to 4.0. Dielectric constant values less than silicon dioxide are typically referred to as "low $\kappa$" films. Any films with dielectric constants less than 3.0 are loosely considered in the industry as being "very low $\kappa$" films. The literature also speaks of "ultra low $\kappa$" films and this loosely applies to films with a dielectric constant of less than 2.0.

Films that have low dielectric constants must meet other requirements for suitable integration into devices. Specifically other key film properties include but are not limited to: (1) breakdown field strength or breakdown voltage, (2) leakage current, (3) thermal stability, and (4) adhesion to other film layers.

Breakdown field strength is expressed in units of volts per unit length and is the point at which an insulating material no longer insulates, breaking down and resulting in a short circuit. The minimum breakdown field strength is determined by dividing the operating voltage of the circuit by the separation distance between adjacent conducting elements. For example, for a 0.25 $\mu$m device having an operating voltage of 3.3 volts, the breakdown voltage must exceed 13.2 volts per micron, or 0.132 MV/cm. A safety margin is desirable, and the industry standard for breakdown field strength for dielectric films is greater than 0.5 MV/cm.

Leakage current is the amount of current flux through an insulator at a specified field

strength that is less than the breakdown field strength. An accepted standard for leakage current density for dielectric films is less than $2\times10^{-8}$ amps/cm$^2$ at an applied electric field strength of 0.05 MV/cm.

If the dielectric strength is sufficiently high (for example, meeting the desired >0.50 MV/cm), and if the leakage current is low enough (for example, meeting the requirement $<2\times10^{-8}$ amps/cm$^2$ at an applied electric field of 0.05 MV/cm), the dielectric layer may be used by itself without the use of other dielectric barriers. However, if the dielectric strength is low (for example, <100 volts per micron) or the leakage current is high (for example, $>10^{-10}$ amps/cm$^2$ at an applied electric field of 0.1 MV/cm), additional dielectric barriers such as a conformal vapor deposited coating of $SiO_2$ or $SiN_4$ may be required.

Combining a thin, high dielectric strength liner such as $SiO_2$ or $SiN_4$ and a low dielectric constant material may provide overall improved dielectric performance. However, the net dielectric constant of the combined dielectric layers is higher than that of the low dielectric constant material itself. The preferred approach is to incorporate a single dielectric material having both low dielectric constant and high dielectric strength to minimize the extra fabrication steps required to include the barrier layer, and to capitalize on the single material's low dielectric constant.

The requirement for mechanical stability at elevated temperatures arises because of the many processing steps that a typical semiconductor wafer undergoes to fabricate the circuitry. The temperatures under which subsequent layers are deposited or processed can reach as high as 400°C. Hence, this value is often used to judge the viability of a film material.

Finally, the adhesive properties of the insulating film must be suitable for subsequent processing as well as ensuring stable thermal and electrical performance. The requirement is thus that the dielectric film bond well with other layers and with the substrate.

Prior art methods of creating thin dielectric films include, for example, chemical vapor deposition (CVD) and spin-on. CVD methods typically apply thermal energy to precursor chemicals and reactants to enable chemical reactions. Other assisted CVD methods may use liquid or plasma to promote the chemical reactions. Often the precursor chemistries are gases, though liquids that are vaporized and injected into a chamber are also used. Alternatively, spin-on methods typically deposit a precursor suspended in a liquid carrier onto a substrate that is

spinning to form a thin uniform film. The coating on the substrate is then cured. The apparatus for spin-on films can be quite simple. However, the classes of chemical precursors, the ability to fill small structural features on substrates, the breadth of film process window and parameters that can be met, and the ability to tailor the resulting film chemistry and properties are better addressed by CVD methods.

A variety of materials have been investigated as low κ dielectric layers in the fabrication of semiconductors. Fluorine has been added to $SiO_2$ films in an attempt to lower the dielectric constant of the film. Stable fluorine doped $SiO_2$ formed by plasma CVD typically has a dielectric constant of 3.5 to 3.7. However, for device geometries well less than 0.25 microns, materials having even lower dielectric constants are desired.

Another plasma CVD approach to create low κ films is the deposition of highly crosslinked fluorocarbon films, commonly referred to as fluorinated amorphous carbons. The dielectric constant of the more promising versions of such films has generally been reported as having a dielectric constant between 2.5 to 3.0 after the first anneal. Problems with fluorinated amorphous carbons remain, however most notably with adhesion, thermal stability (including dimensional stability), and the integration of the films.

Polymeric materials have also been investigated. For example, spin-coated polymeric materials have been employed. Despite their lower dielectric constants, these polymers are not entirely satisfactory due to processing and material limitations. Polymers are generally thermally and dimensionally unstable at standard processing conditions of about 400 to 450°C. While these materials have been considered for embedded structures, as a rule they are not suitable for full stack gap fill or damascene structures.

Because of the disadvantages of spin-coated polymers, vapor phase polymerization has been explored as an alternative method for the preparation of low dielectric constant materials. One particular class of polymers that has been prepared through vapor phase polymerization is the polyxylylenes (also known as parylenes) such as parylene N (ppx-N), and parylene F (ppx-F). Parylenes typically have dielectric constant values ranging from 2.3 to 2.7 and are thus attractive as low dielectric materials for use in integrated circuits. However, the parylenes that have been prepared to date exhibit poor thermal stability as with ppx-N; expensive as with ppx-F; or have poor mechanical stability.

As indicated in the discussions above, fluorinating materials typically reduce the overall dielectric constant value. One material having a very low dielectric constant is polytetrafluoroethylene (PTFE), with a dielectric constant of about 1.9. More recent developments have sought to lower materials with modest dielectric constants by making them more porous; that is, incorporating the low dielectric property of air into the film. The higher the porosity of the material is, the lower is its dielectric constant. However, high porosity materials will tend to be structurally more fragile, and may not meet planarization requirements. Further, materials containing fluorine have the disadvantage of requiring the addition of a barrier layer to minimize fluorine migration during processing and over time.

Unfortunately, materials containing fluorine have the disadvantage of requiring the addition of a barrier layer to minimize fluorine migration during processing and over time. The problem is aggravated in those fabrication processes that use copper, which itself tends to migrate. Barrier layers such as TiN that have been shown to effectively contain fluorine migration, have high dielectric constants, and thus may offset the advantages introduced by the fluorinated film.

More recently, a method of making low dielectric constant films has been described in U.S. Patent No. 6,068,884 where the film is a hybrid of inorganic and organic groups. Such a film and method looks promising, and further development is desirable.

In summary, as demonstrated above, many considerations are required in choosing a low dielectric constant film. There is a continuing need to develop improved systems and methods for depositing low dielectric constant films.

## Summary of the Invention

Accordingly, it is an object of the present invention to provide an improved system and method for depositing low dielectric films. In one broad aspect of the invention a system for depositing a dielectric film on the surface of a substrate is provided having a processing chamber with a substrate support for supporting a substrate and one or more gas inlets for conveying gases to the processing chamber. A first plasma source defining a first plasma zone within the chamber is provided, and a second plasma source defining a second plasma zone within said chamber is provided. Gases are separately ionized at different ionization levels in the first and

second plasma zones, and these separately ionized gases react to form a dielectric film on the surface of the substrate.

In another aspect of the present invention, a method is provided of depositing a dielectric film on the surface of a substrate in a processing chamber wherein one or gases are conveyed to the processing chamber. Any one of, or combination of, the one or more gases are ionized in a first plasma zone. Any one of, or combination of, the one or more gases are separately ionized in a second plasma zone. These separately ionized gases are reacted to form a dielectric film on the surface of the substrate.

## Brief Description of the Drawings

Other objects and advantages of the present invention will become apparent upon reading the detailed description of the invention and the appended claims provided below, and upon reference to the drawings, in which:

Figure 1 is a cross-sectional schematic diagram of the system according to one embodiment of the present invention.

Figure 2 is a cross-sectional schematic diagram of the system according to another embodiment of the present invention.

Figures 3A to 3E are simplified partial schematics showing the system of the present invention according to a number of alternative embodiments.

Figure 4 is a cross-sectional cut away view showing the hollow cathode according to another embodiment of the present invention.

Figures 5A and 5B are a cross-section and bottom plan view, respectively, of a hollow cathode cone according to one embodiment of the present invention.

Figure 6 is a cross-sectional cutaway top plan view of the system according to an alternative embodiment of the present invention.

## Detailed Description of the Invention

Referring to Figs. 1 and 2, where like components are designated by like reference numbers in the figures, two alternative embodiments of the system of the present invention are shown. The system 10 generally includes a processing assembly 11 having a processing

chamber 12, and a hollow tube cathode 14 and a substrate support 16 disposed within the processing chamber 12. A main electrode 18 is positioned adjacent the exterior surface of the processing chamber 12. A top plate 20 seals the upper end of the processing chamber 12, and the hollow tube cathode 14 extends through the top plate 20 into the processing chamber 12. The top plate 20 may include one or more gas inlets 22 for conveying one or more gases to the processing chamber 12. Coupled to the processing chamber 12 is a vacuum system for evacuating the processing chamber 12. As described in further detail below, the vacuum system includes a vacuum plenum and a pump and this vacuum system may be located at the bottom of the processing chamber, or at the top of the processing chamber, or at both locations to provide alternate pumping paths.

As shown in Figs 1 and 2, the processing assembly 11 includes the processing chamber 12 which is cylindrical in shape; however the shape is limited and any suitable shape may be employed. The processing chamber 12 has an exterior wall 24. The exterior wall 24 is preferably made of a low loss insulating material, such as quartz or ceramic. The main electrode 18 is positioned adjacent the exterior wall 24 of the processing chamber. The processing assembly 11 may further include an enclosure 28 surrounding the outer periphery of the processing chamber 12 and the main electrode 18 as shown in Figs. 1 and 2.

The main electrode 18 can take many forms. In one example, the main electrode may be formed of a continuous coil, or a continuous cylinder, that extends along the outer periphery of the processing chamber 12. Alternatively, the main electrode may be formed of a plurality of separate cylindrical sections, which may be spaced from each other at desired intervals around the outer periphery of the processing chamber 12. Preferably the main electrode is a continuous coil. The main electrode 18 should fit tightly over the exterior surface of the processing chamber 12 to maximize the power coupling efficiency from the main electrode 18 to the interior of the processing chamber 12. The main electrode 18 is powered by a conventional power supply 32. Typically, RF powers of up to 3000 Watts at a frequency of 13.56 MHZ are applicable. One example of a main electrode and power supply suitable for use in the system of the present invention are further described in U.S. Patent no. 6,015,595, the entire disclosure of which is herein incorporated by reference.

The hollow tube cathode 14 is disposed within the processing chamber 12 generally via

an opening in the top plate 20. The hollow tube cathode 14 acts as a counter electrode, and is grounded. Alternatively, the hollow cathode 14 can be powered by a conventional power supply 32 and the main electrode can be grounded. Preferably the power supply operates at a frequency of 13.56 MHz, but can be operated at frequencies as low as 1 kHz.

The hollow tube cathode may also serve as a gas inlet to convey one or more gases to the processing chamber 12. The hollow tube cathode 14 is an elongated tube typically having an inside diameter of about 0.25 inches or less, and more usually in the range of about 0.25 to 1.0 inches. In the preferred embodiment the hollow tube cathode is located centered along the center axis of the chamber 14; however, the cathode 14 may be off-set from the center if desired. Thus, one can selectively control the points of entry of the processing chemicals by the location of the hollow tube cathode 14.

The top plate 20 includes a flange 35 around the peripheral edge of the top plate that is secured to the enclosure 28 to seal the top of the processing chamber 12. The top plate 20 includes one or more gas inlet ports for conveying one or more gases to the processing chamber 12. For example, in an exemplary embodiment a first gas inlet port 22 is formed in the top plate 20 and is coupled to a first gas source 38. Many types of chemical gases may be conveyed to the processing chamber 12, and include but are not limited to precursors or reactants, inert gases, carrier gases, or cleaning chemicals. A flow control device 40 is coupled between the gas inlet port 22 and the first gas source 38 to meter the delivery of gases repeatably to the chamber. Commercially available flow control devices suitable for metering of the gases include mass flowmeters (MFM), mass flow controllers (MFC), and direct liquid injection systems. In the case for chemicals that are liquids, liquid delivery systems (not shown) that vaporize the chemical(s) are required. Commercially available liquid delivery systems include vaporizing liquid delivery systems and bubbler systems in which a carrier gas is bubbled through the liquid chemical.

Disposed within the processing chamber 12 is the substrate support 16 which support as substrate, such as a semiconductor substrate or wafer 42, to be processed. Preferably the substrate support 16 is substantially aligned with the center axis of the processing chamber. The substrate support 16 is located near the bottom of the processing chamber 12, below the gas inlets and hollow tube cathode. To hold the wafer 42 firmly within the processing chamber 12

and to minimize the amount of deposition behind the wafer, electrostatic force may be applied to the wafer by the support 16. Any suitable conventional substrate support or chuck may be employed with the present invention. Usually a dc voltage supply (not shown) is used to provide electrostatic clamping of the wafer. While electrostatic clamping of the wafer with an electrostatic chuck is preferred, other types of supports or chucks may be used. Temperature control means, such as cooling fluids, are typically circulated through the support 16 to maintain the support and wafer at desired temperatures. The processing temperatures may be above, or below, room temperature . The substrate support also typically includes a mechanism (not shown) that transfers the wafer to/from the substrate support that is attached to the chamber assembly 11. The mechanism is usually comprised of pins that extend and retract above the support 16 to receive and remove the wafer. A wafer transport system (not shown) having a robot arm and end effector are typically used to load and unload the wafers on the substrate support. These features are well known in the art and thus are not further described herein.

The vacuum system is coupled to the processing chamber 12 for exhausting and/or evacuating the system 10. As illustrated in Figs. 1 and 2, the vacuum system may take a variety of alternative forms. In the exemplary embodiment shown in Fig. 1 the vacuum system is comprised of two separate systems 50A and 50B, each located at opposite ends of the processing chamber 12. This feature of the invention provides for the selection of alternate pumping paths which, as described in further detail below, advantageously promotes the tailoring of the deposition process.

In particular, the vacuum system may provide for exhausting the processing chamber 12 at any one of, or alternatively both of, the top or the bottom of the chamber 12. In Figs. 1 and 2, vacuum system 50A is located near the bottom of the processing chamber 12, below the plane of the wafer. Fig. 6 shows a partial, cross-sectional top view of the vacuum system according to this one embodiment of the present invention. Generally, the vacuum system 50A includes a pumping plenum 52, valve 54, and a pump 56. Any suitable pump may be used, such as but not limited to a turbo pump. The valve 54 preferably provides pressure control via a conventional pressure control feedback system (not shown). As shown particularly in Fig. 6 the pumping plenum 52 in this exemplary embodiment is annular and encircles the wafer support to provide substantially uniform gas flow circumferentially over the wafer 42. The pumping plenum 52 is

T-coupled to the valve 54 and pump 56 inlet, which is typically located off-axis for space considerations. The pumping plenum 52 is sized with an inner and outer diameter to provide adequate pumping and pressures. The pumping plenum 52 may be necked down to length and gap dimensions to promote substantially uniform flow around the circumference of the wafer 42. The operational pressures will depend on the type of processing, and typically the vacuum system is designed to operate over a stable and repeatable pressure operating regime of about 10 milliTorr to 100 Torr with gas flowrates of up to about 1000 sccm. The pressure within the processing chamber 12 is measured using a conventional pressure transducer 55 or other suitable pressure measurement means, which is exposed to the processing chamber 12 through a pressure port 57 in an exterior surface of the chamber 12, and coupled to a conventional pressure control feedback system (not shown).

The vacuum system enables substantially uniform pumping through the pumping plenum 52 and then further promotes substantially uniform gas flow by restricting the gas flow/evacuation path circumferentially. In another embodiment as shown in Figure 6, the restriction of gas flows can be further controlled by using a removable annular ring 58 having an offset outer periphery. The offset or eccentric outer periphery provides a gap 59 which may be selectively sized. For example, as shown in Fig. 6, the gap 59 is larger near the pump 56 shown as location "A" and smaller near the wafer transport port 19 shown as location "B." Alternatively, the annular ring 58 may be of other shapes, for example, an oval ring, or any other shape having an eccentric outer diameter.

An alternative vacuum system 50B is illustrated with reference to Figs. 1 and 2. In this embodiment the vacuum system 50B is positioned above the plane of the wafer. This provides for exhausting the gases up through the processing chamber 12. This vacuum system 50B generally includes a pumping plenum 60 in communication with the processing chamber 12, a valve 62 and pump 64. Preferably, the pumping plenum 60 is located along the center axis of the processing chamber 12 to promote substantially uniform and symmetrical removal of the gases. The pumping plenum 60 is attached to the top plate 20 at one end, and to the pump 64 via a T-coupler 65 at its opposite end. Baffles (not shown) may be positioned within the pumping plenum 60 to improve uniformity of the gas exhaust flow as well as to capture and/or control particulate matter that often forms during processing. This helps to prevent such particles from

falling back down into the processing chamber 12 and contaminating the film on the wafer.

In the embodiment where the system 10 includes both vacuum systems, the vacuum systems 50A and 50B can be operated in the alternative, that is one vacuum system may be operating during processing while the other is not. In another embodiment, both vacuum systems 50A and 50B may be operational during processing. In this embodiment, gases are exhausted from both the top and bottom of the processing chamber, and the amount of gas flow exhausted though each system 50A and 50B is controlled as desired by selecting the settings of each of the valves 54 and 62.

To deposit low $\kappa$ dielectric films, and in particular inorganic/organic films, the system of the present invention may be operated in a variety of methods as described below. As used throughout the present description, the term "inorganic/organic" refers to a dielectric film which is comprised of a combination of inorganic and organic groups. A further description of inorganic/organic hybrid films can be found in U.S. Patent No. 6,068,884, the entire disclosure of which is herein incorporated by reference. While the preferred embodiment is directed to a method of depositing inorganic/organic dielectric films due to their low $\kappa$ properties, the present invention is in no way limited to the deposition of such films, and instead can be employed to deposit other desired dielectric films.

The inventors have developed a unique system and method for depositing low $\kappa$ dielectric films on the surface of a substrate. Traditionally, plasma based deposition systems are designed to deliver a silicon containing material (such as silane, trimethylsilane (TMS) trimethoxysilane, or tetraethoxysilane (TEOS)) to the surface of a silicon wafer in a uniform laminar type flow pattern. The prior art approach has focused on retrofitting high density plasma systems that are designed to produce highly ionized plasmas that dissociated as completely as possible the silicon containing precursor. The silicon is then typically reacted with oxygen to grow highly inorganic silicon dioxide thin films. As described in the aforementioned background however, these approaches have proven to be of limited success, and have been unable to repeatably produce films with low dielectric constants such as below 2.7.

Contrary to the teaching of the prior art, the present invention seeks to minimize ionization of the precursors. Further the present invention promotes the direct flow of ionized gases over the wafer surface. This is accomplished by providing two substantially distinct

plasma zones within the processing chamber 12. In a broad aspect the present invention provides the processing chamber 12 with a first plasma source defining a first plasma zone 66 within said chamber; and a second plasma source defining a second plasma zone 68 within said chamber. Gases conveyed to the processing chamber are separately ionized in the first and second plasma zones, and these separately ionized gases react to form a dielectric film on the surface of said substrate. The gases may be ionized at different ionization levels within the two plasma zones.

Specifically, the first plasma source, which in this embodiment is selected to be the main electrode 18, when powered creates a first, upper plasma zone 66 in the bulk of the processing chamber 12. The second plasma source, in this embodiment selected to be the hollow tube cathode 14, when powered creates a second, lower plasma zone 68 in the region adjacent the surface of the wafer. The upper zone 66 is substantially isolated from the surface of the wafer and a more highly ionized plasma may be generated in this region. This upper zone with its more highly ionized plasma can produce ionized neutral species, such as for example excited argon atoms, which are then extracted by the exhaust gas flow and diffusion to the lower plasma zone 68 which is less highly ionized than the upper zone 66. Preferably, the lower plasma zone 68 is defined by the region around the distal end 67 of the hollow tube cathode 14, and extending down to the surface of the wafer. In an alternative embodiment, a cone 70 as described further below, is placed on the distal end of the hollow tube cathode 14 to further define and direct the shape of the lower plasma zone 68. Additionally, the pitch, length and/or placement of the cone 70 may by varied to create a third plasma zone as described below.

To create the plasmas in the different plasma zones, one or more gases are conveyed to the processing chamber 12. Gases are conveyed through one or more gas inlets 22, and optionally additionally though the hollow tube cathode 14. For convenience the gas inlets 22 are typically formed in the top plate 20, however this is not a requirement and gas inlets may be positioned in other suitable locations.

Of particular advantage, the present invention provides for a variety of chemical delivery options as now described and illustrated in FIGS. 3A to 3E. In addition to the gas inlets 22, gaseous chemical(s) may be conveyed through the hollow tube cathode 14 and into the processing chamber 12. By introducing gases through the cathode 14, the gases are isolated from the larger volume of the processing chamber 12 and its upper plasma zone 66, and instead are

directed to a specific area closer to the surface of the substrate. Further, the gases are separately ionized in the hollow tube cathode 12 in the lower plasma zone 68. These two plasma regimes, the upper plasma zone 66 of the large volume of the chamber and the lower plasma zone 68 within the cathode and the region adjacent the wafer, allow one to selectively control the degree of ionization of the various gases by selecting the region where such gases are introduced into the chamber.

In one exemplary embodiment, an inert gas such as argon is conveyed to the chamber via inlet 22 located in the top plate 20. The argon atoms are ionized in the upper plasma zone 66 by the main electrode 18. A silicon containing precursor or reactant gas such as an organosilicon, and any needed carrier gas, is conveyed through the hollow tube cathode 14. The precursor is ionized as it travels through the cathode and as it exits in the lower plasma zone 68. The precursor interacts with the ionized inert atoms from the upper plasma zone 66, and with pumping action away from the wafer surface provided by the vacuum system, promotes the deposition of a film on the surface of the wafer that is controlled in terms of structure and composition. This allows the deposition of films that preserves, at least in part, the precursor structure. For example, if the precursor is a cyclic organosilicon, the present invention provides for depositing a film wherein the chains or rings of the organosilicon precursor structure are present in the film, and the presence of the plasma cross-links the components to form a continuous thin film with polymeric and ceramic features, structures and performance. The use of the different plasma zones according to the present invention provides for different ionization levels of the gases exposed to each of the plasma zones and promotes this advantageous deposition. Further, this advantageous deposition is achieved without the need for heating the process. The inventive system and method promote relatively "long lived" excited reactant species which possess enough energy to cause the reactions, without requiring external heating.

Alternatively, the silicon containing precursor may be conveyed to the chamber via a different gas inlet, such as gas inlet 22 in the top plate 20 of the processing chamber 12. In this embodiment, the precursor is ionized in the upper plasma zone. Inert gas, such as argon, may be conveyed through the hollow tube cathode 14. Optionally, a portion of the precursor may be conveyed though the hollow tube cathode 14 and thus ionized in the lower plasma zone, and the remaining portion through the gas inlet 22 to be ionized in the upper plasma zone. In general, the

chemical structure and the resulting bond energies of the gases will determine the degree of ionization required, and therefore the desired injection location for the gases.

In the embodiments shown in FIGS. 1 and 3A to 3B, the lower plasma zone 68 is defined by the position of the distal end 67 of the hollow tube cathode. The hollow tube cathode 14 is positioned adjacent the surface of the substrate. Preferably the cathode 14 is positioned above the substrate support and is centered along the axis of the chamber 12. The distance between the distal end 67 of the hollow cathode 14 and the surface of the substrate may vary from almost zero to about 10 inches, and more usually between about 3 to 6 inches, with a distance of about 3 inches being most preferred. The diameter of the hollow tube cathode may be of any suitable size depending on the desired gas flow rates and pressure, and preferably size of the hollow cathode may vary up to about 1 inch outer diameter, with up to about 0.90 inches inner diameter.

As mentioned above, in another aspect of the present invention, a cone 70 as illustrated in FIGS. 2, 3D-3E and 5A-5B is employed to further define the geometry or region of the second or lower plasma zone, or alternatively may be employed to define a third plasma zone 72. To create a third plasma zone 72, the cone can be powered by a conventional power supply or grounded, and is typically electrically coupled to the hollow tube cathode 14. Specifically, the cone 70 is placed along the distal end of the hollow tube cathode 14 to create the third plasma zone 72, which is defined as the volume within the cone but outside of the hollow tube cathode 14. In this embodiment, the second or lower plasma zone 68 is defined as the volume inside the hollow tube cathode and at the exit of the cathode 14. The pitch 71 and diameter 73 of the cone 70 will determine the relative intensities of the plasmas in the second and third zones, and thus also the degree of ionization occurring in each zone or regime. The cone 70 may be placed at the distal end 67 of the hollow tube cathode 14 as shown for example in FIG. 3E, or further up the cathode away from the distal end as shown in FIG. 3D.

The size of the cone 70 may vary considerably, and the cone 70 may have pitch up to the same as the height of the plasma chamber 12, and have a diameter that is just less than the diameter of the plasma chamber 12. In one example, the diameter 73 of the cone 70 may range from about 7 to 10 inches, and the pitch 71 of the cone 70 may range from about 1 to 7 inches. When processing an eight inch diameter wafer 42, a cone diameter 73 of about 9 inches and a pitch 71 of about 1 inch is preferred. The shape of the cone may also vary, for example it may be

a simple cone as shown in FIGS 3D and 3E, the cone 70 may be shaped of a single ended hollow cylinder 74 as illustrated in FIG. 5.

Thus, when the cone 70 is powered, a gas passing though the hollow tube cathode 14 will be exposed to two separate plasma zones. Direct dissociation of the gas is achieved in the hollow tube cathode and further dissociation is achieved within the cone. Of particular advantage, the introduction of the cone 70 enables yet another means to control the ionization of the precursor gases; and more specifically, the regime in which the ionization takes place. By controlling the degree and location of ionization, the present invention provides for better control of the desired dielectric constant in the resultant film, as well as the film uniformity over the large surface area of the wafer.

To selectively ionize and dissociate the gases, power is supplied to either the main electrode 18 or the hollow tube cathode 14 via power supply 32. Conventional plasma systems are designed to highly ionize the gases which create dense films on the wafer, and these dense films have a high dielectric constant. Conversely, the inventors have discovered that by employing a lesser amount of power, films may be deposited having a low dielectric constant. Suitable applied power ranges according to the present invention will vary depending on the size of the wafer, and the exact equipment configuration, and such power ranges can be obtained by routine experimentation based on the teaching of the present invention. In one example, the applied power range is typically less than 500 watts, and more preferably at about 300 watts for an eight inch wafer and a plasma source volume of about 900 $in^2$. Additionally, unlike HDP or similar conventional plasma systems that require the wafer surface temperature exceed about 100 °C, the present invention provides for carrying out the deposition process at or near room temperature. This is possible, since all the energy needed to promote the necessary reactions is provided by the plasma state.

During processing of the wafer, the processing chamber 12 may be exhausted from either the top, the bottom, or both; however, exhausting from the top of the chamber has been found to be preferred. In either case, as described above the exhausting of the gases is preferably on-axis; that is, symmetrical about the center axis of the chamber to promote substantially uniform flow of the gases about the surface of the substrate. Substantially uniform flow of the gases about the surface of the substrate promotes the deposition of a more uniform film. Selection of the

particular pumping path may vary with the type of processing desired.

In another aspect of the present invention, a method for depositing low dielectric constant films on the surface of substrates is provided. As described in the foregoing background, many prior art methods used achieve low-κ ( i.e. <3.0) dielectric constant materials from PECVD have required fluorine doping of SiOx. Spin-on coatings have demonstrated good performance, but have many limitations. A PECVD material with κ<3.0 and no fluorine is highly desired. In particular the system achieves films exhibiting dielectric constants of less than 3.0, and preferably equal to and less then about 2.7. Dielectric constants as low as about 2.5 have also been achieved with the system of the present invention. The present invention provides for using an organosilicon precursor and ionizing/activating the precursor at an energy level such that it is not highly dissociated thereby the original chemical structure of the precursor is preserved, at least in part, in the final film deposited on the wafer.

The present invention provides controlling the point of ionization/activation of the precursor material in relationship to the silicon wafer surface and the point at which volatile byproducts, such as water and hydrocarbon materials in addition to carbon mono (and di) oxide are removed from the system. The inventors have shown that a low dielectric constant film will preferably have low density, cross-linked silicon-and-oxygen based composition with a low occurrence of OH groups. To achieve such low density, cross-linked, silicon-and-oxygen-based dielectric films with the minimal amount of OH groups, the inventors have discovered that deposition of the film should take place after ionization/activation of the precursor and after gas phase reactions have been accomplished to generate the byproduct reactions. Unlike prior systems and methods which seek to minimize any gas phase reactions and are focused on 100% (theoretically not possible) ionization of the starting materials; the present invention promotes only activation of the precursor materials to a level that the films can be grown, instead of trying to achieve 100% ionization.

Additionally, prior art systems and methods operate at the lowest possible pressures to ensure that there is no gas phase nucleation and that the film formation can only happen at the silicon surface. In contrast, the present invention operates at the highest possible pressures to activate gas phase reactions, which will result in film formation at the silicon surface from agglomerated groups in the gas phase - this leads to highly porous structures and desirable low k

properties. To accomplish this, the present invention provides for operating at pressures that allow the optimal gas phase nucleation to take place and still allow a film to form on the silicon wafer that has good adhesion and structural integrity.

More specifically, the method of the present invention provides for depositing a low dielectric constant film comprised of inorganic and organic materials or groups. Organosilicon precursors are employed with the method of the present invention. Suitable organosilicon precursors that may be employed in the present invention are further described in U.S. Patent No. 6,068,884, the disclosure of which is incorporated herein in its entirety. In one embodiment, the organosilicon precursors have the general formula of :

$$R_nSi(OSi)_mX_{(2m-n+4)} \quad (1)$$

where n is 1 to (2m+4); m is 0 to 4; the organosilicon may be linear or branched; X is selected form the group consisting of H, and the halogens; and R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons, with and without an oxygen linkage. Examples of suitable aliphatic, olefinic, and aromatic hydrocarbon groups include methyl, ethyl, propyl, butyl, and phenyl, etc.

In another embodiment, the organosilicon precursor may be comprised of cyclic organosiloxanes of the formula:

$$R_n\overline{(SiO)_m}X_{(2m-n)} \quad (2)$$

where n is 1 to 2m; m is 3 to 10; X is selected from the group consisting of H and the halogens; and R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons as listed above.

In yet another embodiment of the present invention, the organosilicon precursor is comprised of organosilazanes of the formula:

$$R_nSi(NSi)_mX_{(3m-n+4)} \quad (3)$$

where the organosilazane may be linear or branched;, and n is 1 to (3m+4); m is 1 to 4; X is selected from the group consisting of H and the halogens; R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons.

In yet another embodiment of the invention, the organosilicon precursor is comprised of cyclic organosilazanes of the formula:

$$R_n\overline{(SiN)}_m X_{(3m-n)} \qquad (4)$$

where n is 1 to 3m; m is 3 to 10; X is selected from the group consisting of H and the halogens; R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons.

Thus, suitable precursors according to the invention include but are not limited to: organic siloxanes, fluorosiloxanes, cyclosiloxanes, fluorine containing cyclosiloxanes, organosilazanes, fluorosilazanes, cyclosilazane, silicates, TEOS, and TMS and mixtures thereof. Examples of suitable side groups include: -H, $-CH_3$, -F, $-C_2H_5$, $-CF_3$, $-C_2F_5$, $-C_6H_5$, $-C_6F_5$, $-CF_2CF_3$, and $C-H_2CF_3$. Combinations of chemicals that when mixed in a reactor could create similar chemical constituents in final form as the aforementioned precursors, for example a mixture of: silane, silicon tetra fluoride and an organic precursor are also suitable.

Of particular advantage, the present invention provides for minimizing the fragmentation of the precursor, thus preserving the general structure deposited in the film. Thus, precursors with components that form a film structure having an inorganic backbone with organic side groups may be used. Examples of organosilicon precursors that are suitable according to the invention include hexamethyl disiloxane (HMDSO), 1,1,3,3-tetramethyldisiloxane (TMDSO) and the like. Other organosilicon precursors such as tetraethyoxysilane (TEOS) may also be used. The materials mentioned are generally inexpensive and readily available. These materials are volatile when heated and thus can be introduced into a plasma CVD reactor system.

In an alternative embodiment, the film of the invention having the ring and chain structure is formed by cyclic organosilicon or cyclic organosilazane precursors. The cyclic organosilicon or organosilazane may be substituted with one or more fluorine atoms. Further, they may be saturated or unsaturated. Examples of suitable cyclic organosilicons include: cyclosiloxanes such as

octamethylcyclotetrasiloxane (OMCTS), hexa methyl cyclo trisiloxane, hexa phenyl cyclo trisiloxane, octa phenyl cyclo tetrasiloxane, 1,3,5-trimethyl-1,3,5-tris-3,3,3-trifluoropropyl cyclo trisiloxane, fluorine containing cyclosiloxanes, and combinations of chemicals that create the same chemical components as above. Organosilazane precursors may also be used. Most preferably, the precursor is octamethylcyclotetrasiloxane (OMCTS).

The organosilicon precursor is conveyed to the processing chamber at a flow rate in the range of about 0.05 to 5.0 cc/min more usually in the range of about 0.05 to 1.0 cc/min with a flow rate of about 0.3 cc/minute being most preferred. Argon gas is also typically added to the chamber at a flow rate in the range of about 0 to 8 sccm. The chamber pressure is generally in the range of about 10 to 1000 mTorr during processing, with a pressure of about 50 m Torr being preferred. The plasma source in one embodiment the main electrode 18, typically has inside dimensions of about 8 inches tall with a 12 inch diameter.

The starting material structure determines whether the organosilicon will be suitable for creating a low-κ material. In one example, the liquid organosilicon is injected into a previously evacuated chamber at approximately 10 sccm (standard cubic centimeters per minute). No additional gases are added to the organosilicon. The organosilicon material is delivered through the hollow tube cathode 14, with its distal end 67 positioned at a distance of about 3 inches from the surface of the substrate 42 (to minimize the ionization/fragmentation of the material prior to deposition). By controlling the process plasma at low power (in this example at <300 watts for a 200mm wafer) and at high pressure (in this example >25mTorr) a dielectric constant below 3.0 is achieved while maintaining thermal loss (weight %) of <1.0%. It is desirable to ignite the plasma with only the organosilicon material in the gas phase. Once the deposition time has been reached, the power supply is turned off and then the gas flows are terminated and the chamber is evacuated before the wafer is removed and the next wafer is introduced.

In another exemplary embodiment, the inventive method is carried out as follows: A wafer is loaded into the system (once evacuated to vacuum from atmospheric pressure). Gas(es) is conveyed into the processing chamber either through the hollow tube cathode, or through the gas inlet, or through both the hollow cathode and gas inlet. The point of entry of the gas depends on the desired film properties of the film that will be deposited onto the semiconductor wafer. For example, if one desires a highly cyclic, porous SiOC film, octamethylcyclotetrasiloxane may be delivered

through the hollow cathode, or through the gas inlet. A plasma is ignited in the main electrode and plasmas are established in a plasma zone at the tip of the hollow cathode (if pressures above 25 mTorr are selected) and in another plasma zone in the general volume of the processing chamber. Gas flows and pressures are selected to ensure that a significant amount of SiOC material is deposited onto the semiconductor wafer. The effluent gases are evacuated from the chamber via the pumping plenum coupled to the top of the processing chamber.

In another aspect of the invention, a nanocomposite material may be deposited, for example a SiOC film as described above but with an additional material dispersed through the bulk of the film such as Teflon™, or any other suitable material. A similar method is carried out as described above, except that the additional material is placed within the hollow tube cathode. In the exemplary embodiment where a composite film having Teflon is desired, the hollow tube cathode is either made out of Teflon or the typically metallic cathode is fitted with a Teflon insert. In one example the Teflon insert has a minimum inside diameter of about 0.125 inches. Argon gas is conveyed through the hollow cathode and a precursor such as octamethylcyclotetrasiloxane is conveyed through the gas inlet at ratios to achieve the desired pressure and film deposition on the wafer. In one example the ratio of argon to octamethylcyclotetrasiloxane is about 1:1. The hollow cathode discharge in the end of the hollow cathode is selected to be sufficient to ionize and sputter the Teflon from the insert or solid Teflon pipe. The discharge may be observed by monitoring the optical emission profile.

In another aspect of the present invention, a method is provided wherein hydrogen (H) abstraction is performed to deposit low dielectric constant SiOC films. H-abstraction leaves much of the original precursor structure in tact. Specifically, a hydrogen atom is abstracted from a labile group such as Si-H, using atoms such as $F^-$, $F_2$, O, $O_2$, H, and the like. Hence, instead of using a fully methylated organosilicon precursor such as octamethylcyclotetrasiloxane (OMCTS), a partially methylated molecule such as tetramethylcyclotetrasiloxane (TMCTS ) is used to generate a free radical on the cyclic siloxane. This free radical initiates chemical reactions leading to film formation.

Because HF has a very high bond strength, $F_2$ can be used in the hydrogen abstraction. Alternatively, a reactive atom or free radical, such as $F^-$, $H^-$, or O, or an electronegative molecule such as $O_2$ , can be used to initiate free radical formation on the organosilicon precursor.

Trends reported in the references cited suggest that an optimum composition may exist in an amorphous organosilicon (SiCO) film for producing the lowest possible κ (dielectric constant) in a nonporous (fully dense) film. That optimum is given by a carbon to silicon (C/Si) ratio of about 3/1, and an oxygen to silicon (O/Si) ratio of about 2:1.

## Experimental

A number of experiments are provided below. These experiments are provided for purposes of illustration only and are not intended to limit the scope of the present invention in any way.

Experiments were conducted to characterize the hollow cathode source. For each condition, "pieces" of a silicon wafer (at least 0.5" square) were placed on a dummy wafer. In addition, glass slides were coated and placed with tape mask to create steps for measuring thickness using a Dektak profilometer. The experimental testing conditions are shown in Table 1 below:

Table 1

| *Hollow Cathode Diameter* | *Hollow Cathode Distance to Wafer* | *Organosilicon Flow (OMCTS) (ccm)* | *Pressure (mTorr)* | *Power (watts)* |
|---|---|---|---|---|
| USE THE HOLLOW CATHODE AS THE GAS INLET THEN: | | | | |
| 0.375" | 6 | 0.4 | 50 | 250 |
| 0.375 | 3 | 0.4 | 50 | 250 |
| 0.375 | 9 | 0.4 | 50 | 250 |
| | | | | |
| 0.25" | 6 | 0.4 | 50 | 250 |
| 0.25 | 3 | 0.4 | 50 | 250 |
| 0.25 | 9 | 0.4 | 50 | 250 |

USE THE SHOWER HEAD AS THE GAS INLET FOR Octamethylcyclotetrasiloxane THEN:

| | | | | |
|---|---|---|---|---|
| 0.375" | 6 | 0.4 | 50 | 250 |
| 0.375 | 3 | 0.4 | 50 | 250 |
| 0.375 | 9 | 0.4 | 50 | 250 |
| | | | | |
| 0.375" | 6 | 0.4 | 100 | 250 |
| 0.375 | 3 | 0.4 | 100 | 250 |
| 0.375 | 9 | 0.4 | 100 | 250 |
| | | | | |
| 0.375" | 6 | 0.4 | 100 | 350 |
| 0.375 | 3 | 0.4 | 100 | 350 |
| 0.375 | 9 | 0.4 | 100 | 350 |

The process conditions employed carrying out the method of the present invention according as illustrated in Table 1 above are:

Organosilicon Flow : about 0.3 ccm

Pressure: about 50 mTorr

Power : about 250 watts

Hollow Cathode Dia: about 0.375 (3/8")

Distance of the hollow cathode to wafer: about 3"

Additional experiments were conducted wherein argon gas was supplied to the processing chamber 12 through the gas inlet 22 in the top plate 20 and octamethylcyclotetrasiloxane (OMCTS) was delivered through the hollow cathode tube 14. The distal end 67 of the hollow tube (cathode) 14 was positioned at approximately 3" from the wafer surface. The process conditions and dielectric constant of the resulting film are shown in Table 2 below. The dielectric constant was determined using a conventional metal dot method for all of the results reported below.

Table 2

| Experiment # | OMCTS (ccm) | Ar (sccm) | Power (watts) | Pressure (mTorr) | Dielectric Constant |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0.28 | 8 | 360 | 50 | <2.5 |
| 2 | 0.24 | 8 | 360 | 50 | >3.1 |

The dielectric constant is founded to vary with the OMCTS flow rate.

Another experiment was conducted where argon gas was supplied to the processing chamber 12 through gas inlet 22 in the top plate 20 and octamethylcyclotetrasiloxane (OMCTS) was delivered through the hollow tube cathode 14. The end of the hollow tube cathode 14 was positioned approximately 6" from the wafer surface. The process conditions and resultant dielectric constant are shown in Table 3 below:

Table 3

| Experiment # | OMCTS (ccm) | Ar (sccm) | Power (watts) | Pressure (mTorr) | Dielectric Constant |
|---|---|---|---|---|---|
| 3 | 0.30 | 8 | 300 | 50 | <2.5 |

Another experiment was conducted where no argon gas was supplied, but octamethylcyclotetrasiloxane (OMCTS) was delivered through the hollow tube cathode 14. A cone 70 was attached to the end of the hollow tube cathode 14 and the end of the cone was positioned approximately 3" from the wafer surface. The process conditions and resultant dielectric constant are shown in Table 4 below:

Table 4

| Experiment # | OMCTS (ccm) | Ar (sccm) | Power (watts) | Pressure (mTorr) | Dielectric Constant |
|---|---|---|---|---|---|
| 4 | 0.28 | 0 | 340 | 50 | 2.5-2.6 |

As described above, an improved system and method for depositing low dielectric constant films on the surface of substrates has been provided. The creation of a plurality of plasma zones formed within the processing chamber, which in combination with the chemical delivery configuration, control the degree of ionization and location of ionization of the precursor chemicals to promote repeatable and uniform deposition of low k dielectric constant films. Further the placement of alternative pumping paths allow the use of an above- wafer plane evacuation path that can draw away unwanted low molecular weight by products from the desired film, or alternatively the use of a below-wafer plane evacuation path that provides

effectively on-axis uniform gas flow across and around the wafer.

The foregoing description of specific embodiments and examples of the present invention have been presented for the purpose of illustration and description. While the present invention has been described with reference to a few specific embodiments, the description is illustrative and is not to be construed as limiting the invention. Various modifications may occur to those of ordinary skill in the art without departing from the spirit and scope of the invention.

We Claim:

1. A system for depositing a dielectric film on the surface of a substrate, comprising:

a processing chamber having a substrate support for supporting a substrate and one or more gas inlets for conveying gases to the processing chamber;

a first plasma source defining a first plasma zone within said chamber; and

a second plasma source defining a second plasma zone within said chamber;

wherein said gases are separately ionized at different ionization levels in said first and second plasma zones, and said separately ionized gases react to form a dielectric film on the surface of said substrate.

2. The system of claim 1 further comprising:

a third plasma zone defined within said processing chamber.

3. The system of claim 1 wherein said second plasma zone is adjacent the substrate support.

4. The system of claim 1 wherein the first plasma source is comprised of an electrode positioned adjacent an exterior wall of the processing chamber.

5. The system of claim 1 wherein the second plasma source is comprised of a hollow tube cathode extending into the processing chamber.

6. The system of claim 5 wherein one or more of the gases is conveyed to the processing chamber through the hollow tube cathode.

7. The system of claim 1 further comprising:

a vacuum system coupled to the processing chamber for exhausting the gases from the processing chamber.

8. The system of claim 7 wherein the vacuum system further comprises:

a pumping plenum disposed in the top of the processing chamber; and

a pump coupled to said pumping plenum to exhaust the gases from the top of the processing chamber.

9. The system of claim 7 wherein the vacuum system further comprises:

an annular pumping plenum disposed in the bottom of the processing chamber and encircling the outer periphery of the substrate support; and

a pump coupled to said pumping plenum to exhaust the gases from the bottom of the processing chamber.

10. The system of claim 9 further comprising an annular ring disposed within said pumping plenum and having an eccentric outer periphery.

11. The system of claim 5 further comprising a cone electrically coupled to the hollow tube cathode, the area inside the cone defining a third plasma zone.

12. A system for depositing a dielectric film on the surface of a substrate, comprising:

a processing chamber;

a substrate support disposed in said processing chamber;

one or more gas inlets for conveying one or more gases into said processing chamber;

a vacuum system having a pumping plenum and a pump coupled to said processing chamber, wherein the gases are exhausted from any one of, or both of, the top or bottom of the processing chamber; and

said processing chamber having a first plasma source for creating a first plasma zone and a second plasma source for creating a second plasma zone,

wherein said one or more gases are separately ionized in said first and second plasma zones, and the separately ionized gases react to form a dielectric film on the surface of the substrate.

13. The system of claim 12 further comprising a cone disposed within said processing chamber and electrically coupled to said one of the plasma sources, the area inside the cone defining a third plasma zone.

14. A method of depositing a dielectric film on the surface of a substrate in a processing chamber, comprising:

conveying one or more gases to said chamber;

first ionizing any one of, or combination of, said one or more gases in a first plasma zone;

second ionizing any one of, or combination of, said one or more gases in a second plasma zone; and

reacting the separately ionized gases to form a dielectric film on the surface of the substrate.

15. The method of claim 14 wherein the gas is ionized at a greater level in said first plasma zone than in said second plasma zone.

16. The method of claim 14 further comprising:

third ionizing any of said one or more gases in a third plasma zone.

17. The method of claim 14 wherein said one or more gases include organosilicons.

18. The method of claim 14 wherein said one or more gases include cyclic organosilicons.

19. The method of claim 14 wherein said one or more gases include octamethylcyclotetrasiloxane.

20. The method of claim 14 wherein said method is carried out at a pressure in the range of about 10 to 1000 mTorr.

21. The method of claim 14 wherein said method is carried out at a pressure of about 50

mTorr.

22. The method of claim 14 wherein said first and second ionization steps are carried out using a plasma source at an applied power in the range of less than about 500 watts for a plasma source volume of about 900 $in^2$.

23. The method of claim 14 wherein said one or more gases are conveyed to the processing chamber at a flow rate in the range of about 0.05 to 5.0 cc/minute.

24. The method of claim 14 wherein the method is carried out at about room temperature.

25. The method of claim 14 wherein at least one of the one or more gases is not highly dissociated during the ionizing steps.

26. The method of claim 14 wherein at least one of said one or more gases is comprised of the general formula of:

$$R_nSi(OSi)_mX_{(2m-n+4)} \qquad (1)$$

where n is 1 to (2m+4); m is 0 to 4; X is selected form the group consisting of H, and the halogens; and R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons, with and without an oxygen linkage.

27. The method of claim 14 wherein at least one of said one or more gases is comprised of the general formula of:

$$R_n\overline{\lfloor(SiO)_m\rfloor}\,X_{(2m-n)} \qquad (2)$$

where n is 1 to 2m; m is 3 to 10; X is selected from the group consisting of H and the halogens; and R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and

aliphatic, olefinic and aromatic fluorocarbons.

28. The method of claim 14 wherein at least one of said one or more gases is comprised of the general formula of:

$$R_nSi(NSi)_m X_{(3m-n+4)} \quad (3)$$

where n is 1 to (3m+4); m is 1 to 4; X is selected from the group consisting of H and the halogens; and R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons.

29. The method of claim 14 wherein at least one of said one or more gases is comprised of the general formula of:

$$R_n\overline{(SiN)_m} X_{(3m-n)} \quad (4)$$

where n is 1 to 3m; m is 3 to 10; X is selected from the group consisting of H and the halogens; R is selected from the group consisting of aliphatic, olefinic and aromatic hydrocarbons, and aliphatic, olefinic and aromatic fluorocarbons.

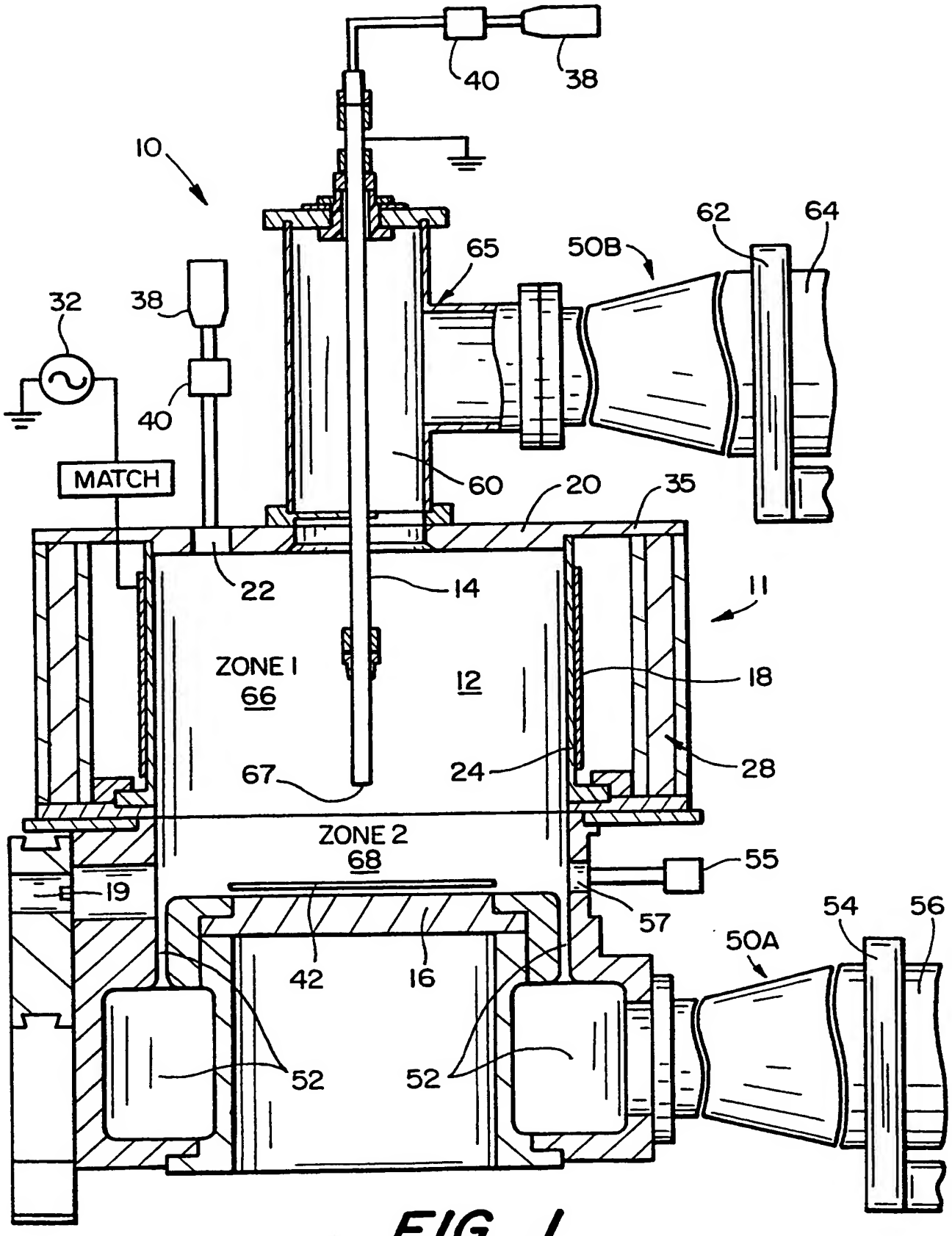
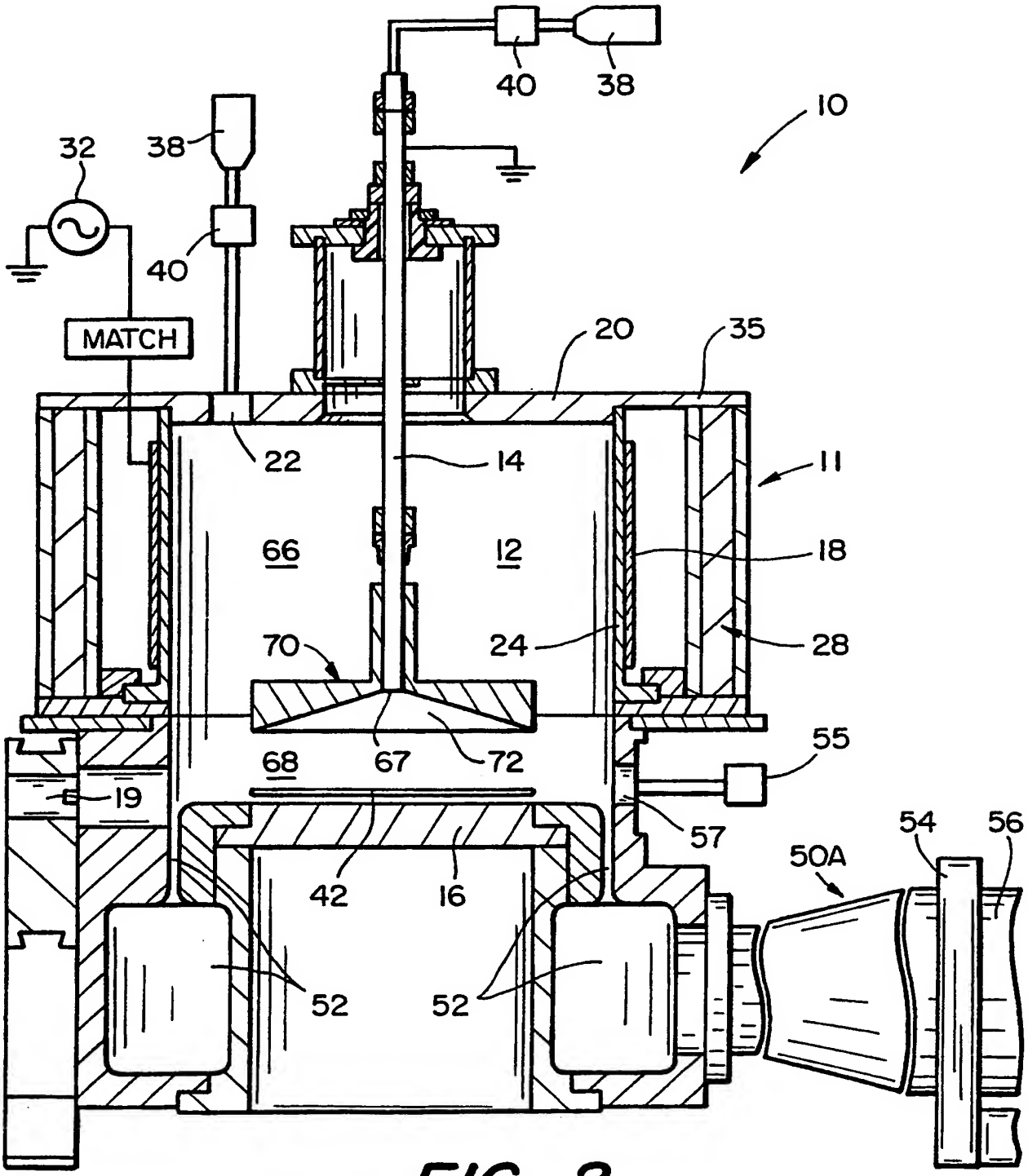



FIG_1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38
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32
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MATCH
20
35
22
14
11
66
12
18
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24
28
55
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67
72
19
57
54
56
50A
42
16
52
52

FIG_2

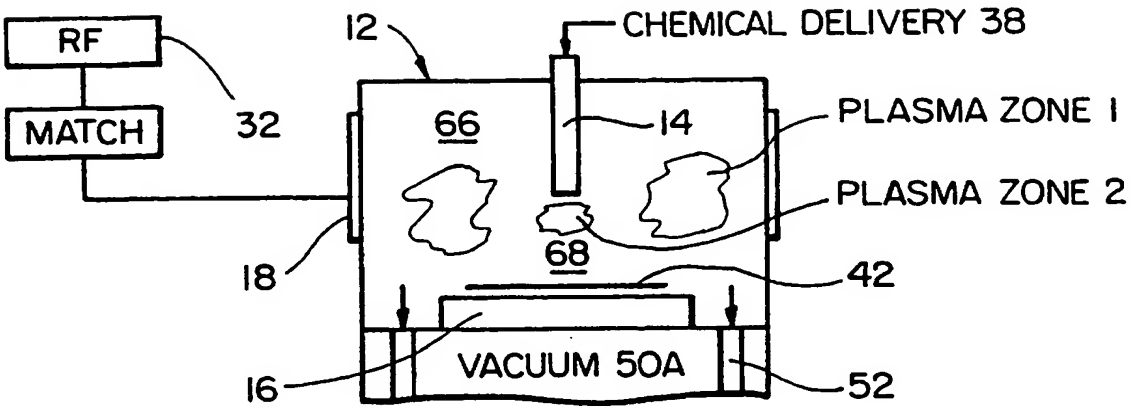



FIG_3A

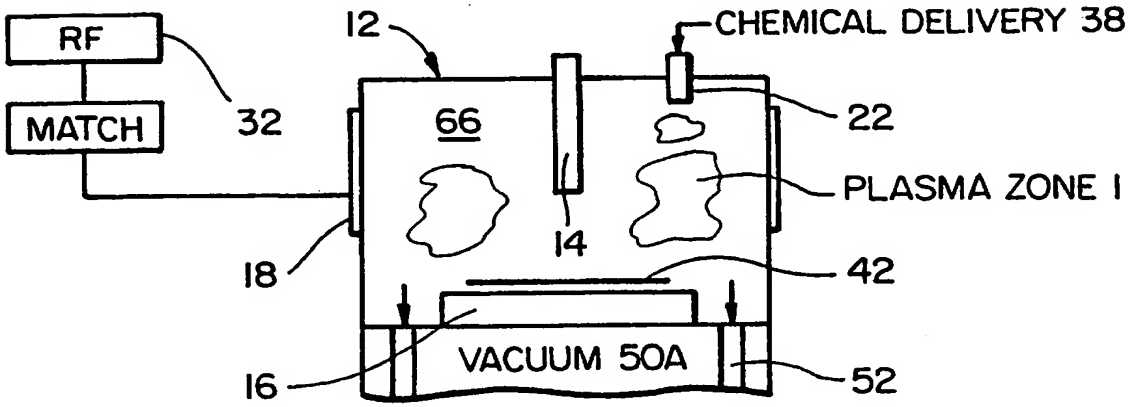



FIG_3B

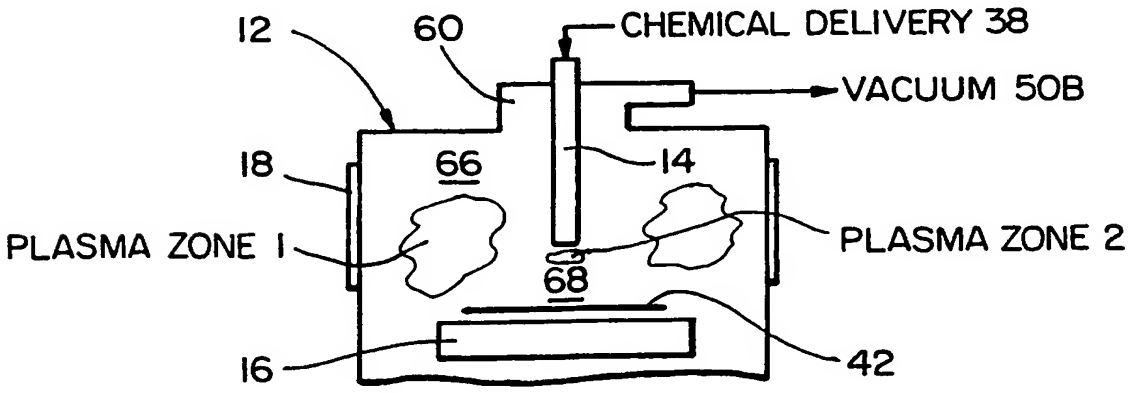



FIG_3C

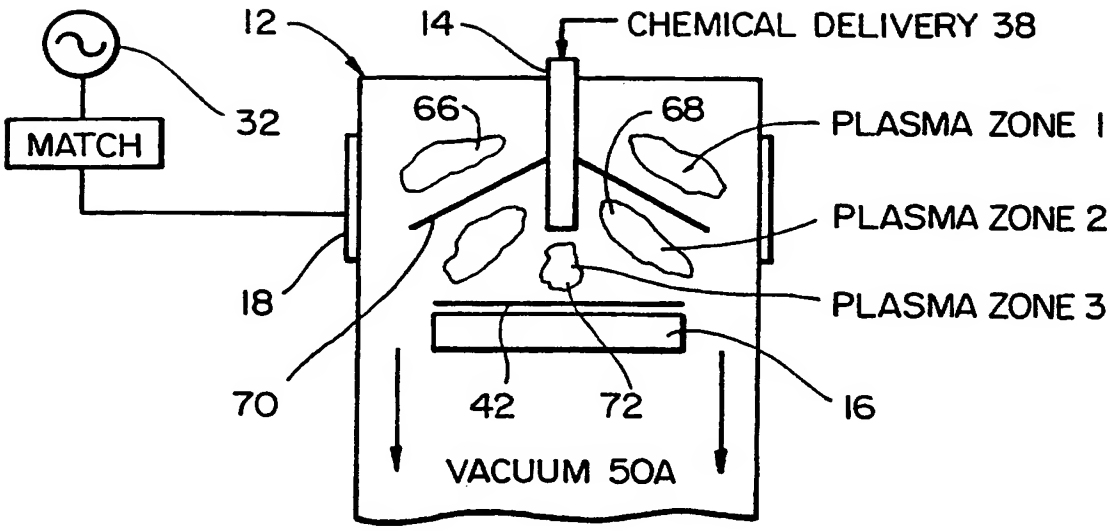
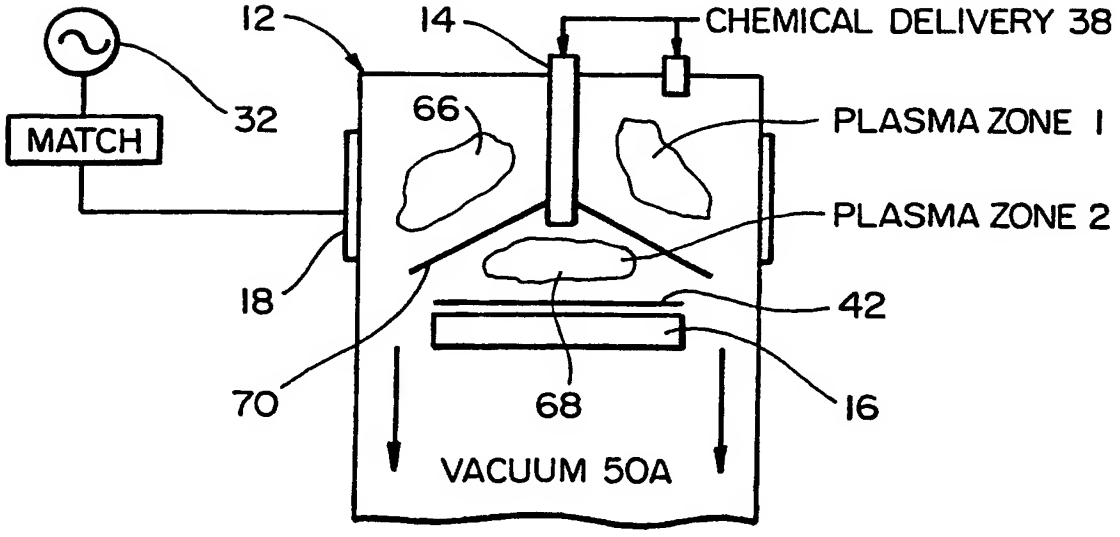

12
14
CHEMICAL DELIVERY 38
MATCH
32
66
68
PLASMA ZONE 1
PLASMA ZONE 2
PLASMA ZONE 3
18
70
42
72
16
VACUUM 50A

FIG_3D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14
CHEMICAL DELIVERY 38
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32
66
PLASMA ZONE 1
PLASMA ZONE 2
18
42
70
68
16
VACUUM 50A

FIG_3E

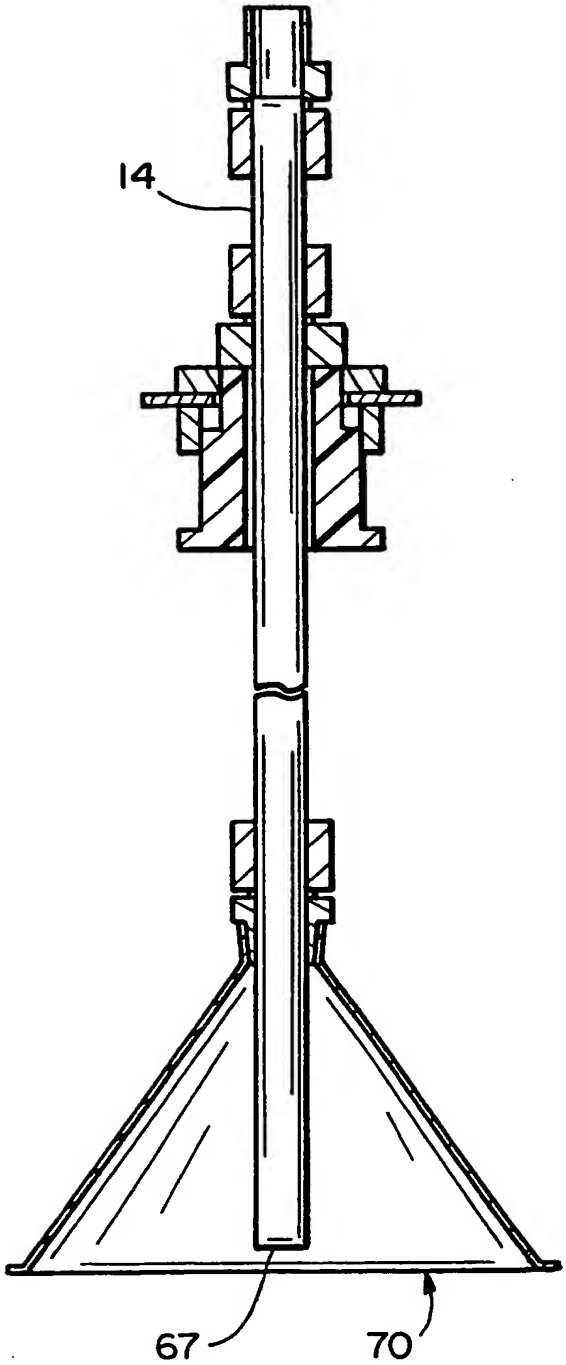


FIG_4

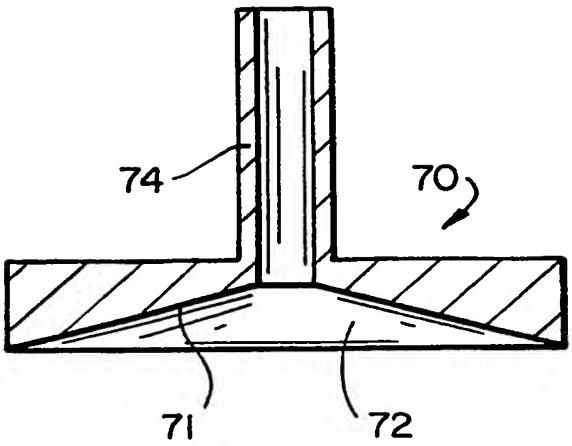


FIG_5A

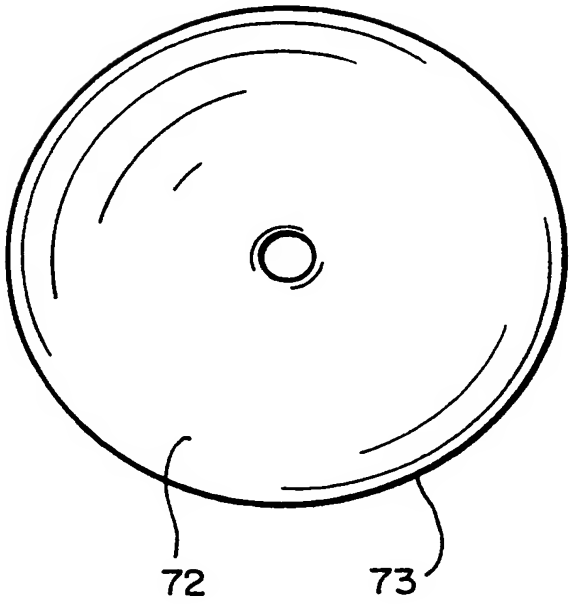


FIG_5B

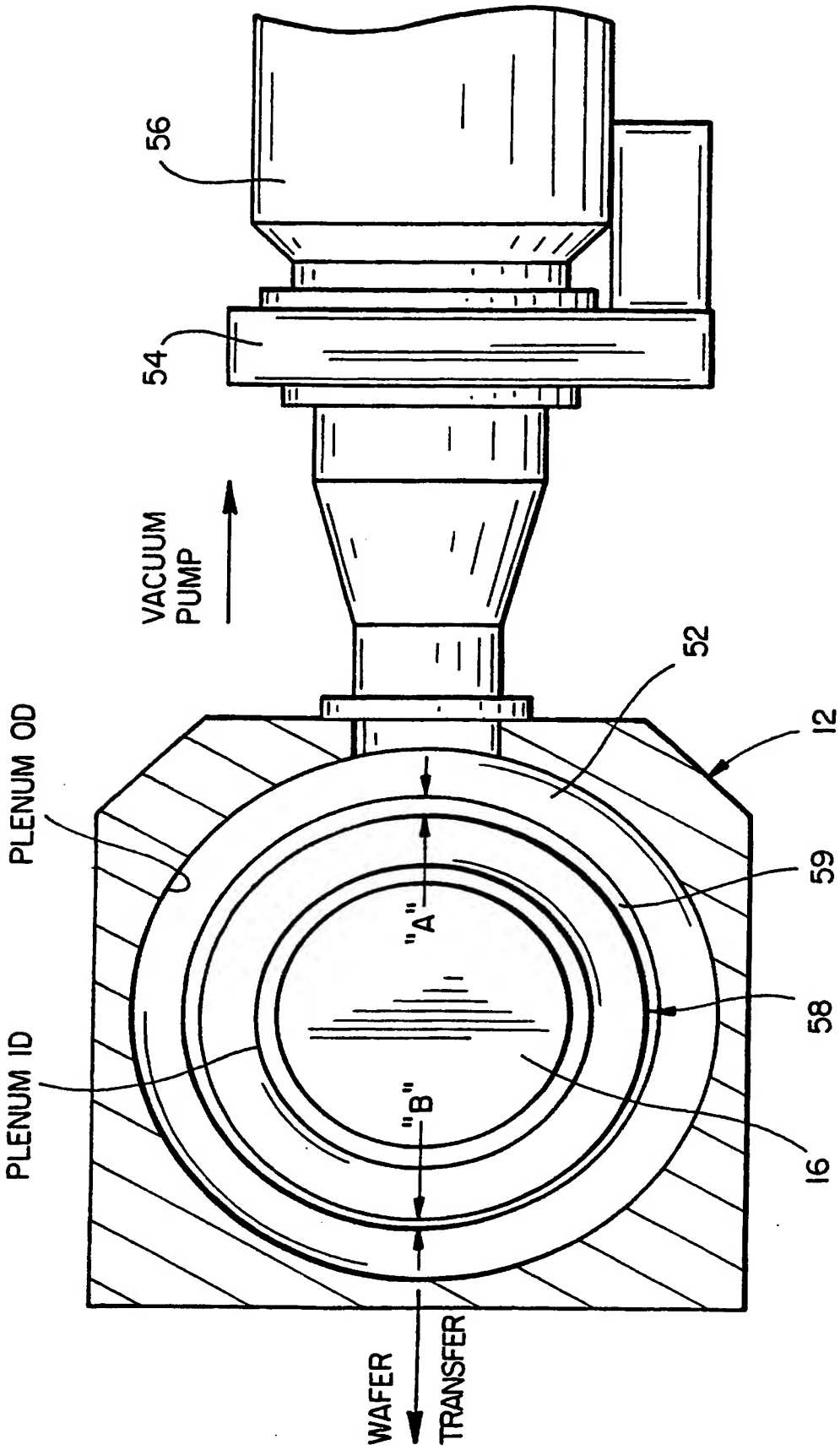


FIG_6

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/31694

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(7) : C23C 16/00; C23F 01/02; H01L 21/31, 21/469
US CL : 156/345; 438/780,781; 118/723E, 723IR, 723ME, 723HC, 715

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 156/345; 438/780,781; 118/723E, 723IR, 723ME, 723HC, 715

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5,695,597 A (FUJIWARA) 09 December 1997, col. 5, line 58 - col. 6, line 42. | 1, 3, 7, 9, 12 |
| X | US 4,948,750 A (KAUSCHE et al) 14 August 1990, col. 3, line 53 - col. 5, line 45. | 1, 3, 7, 12, 14-15 |
| X | US 5,292,370 A (TSAI et al) 08 March 1994, col. 3, line 33 - col.3, line 68. | 1, 3, 7, 9, 12 |
| X | US 5,851,600 A (HORIIKE et al) 22 Decenber 1998, col. 3, line 65 - col. 5, line 56. | 1, 3, 7, 12 |
| A,E | US 6,176,198 B1 (KAO et al) 23 January 2001, see entire document. | 1-29 |
| A | US 5,273,609 A (MOSLEHI) 28 December 1993, see entire document. | 1-29 |

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

| | |
|---|---|
| * Special categories of cited documents: | |
| "A" document defining the general state of the art which is not considered to be of particular relevance | "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
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| "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| "O" document referring to an oral disclosure, use, exhibition or other means | |
| "P" document published prior to the international filing date but later than the priority date claimed | "&" document member of the same patent family |

| | |
|---|---|
| Date of the actual completion of the international search<br>08 FEBRUARY 2001 | Date of mailing of the international search report<br>22 MAR 2001 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>LUZ L. ALEJANDRO<br>Telephone No. (703) 308-0661 |

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/31694

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 5,935,455 A (GLEJBOL) 10 August 1999, col. 4, line 49 - col. 5, line 11. | 1-29 |
| X,P | US 6,015,595 A (FELTS) 18 January 2000, col. 3, line 30 - col. 12, line 8. | 1-29 |

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